ARTIST

Network of Excellence on Embedded Systems in the IST 6th Framework Programme

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Reinhard Wilhelm

Industrial Requirements for WCET Tools

Answers to the ARTIST Questionnaire

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Respondents

- Answered by 12 participants ☹
- Functions: Developers, Engineers, Managers, CTO R&D, Director, Program Manager, Chief Scientist ☺
- Responsible for groups of size:
  - 1-5 9x
  - 6-10 1x
  - 21-100 2x

For which applications/systems do you need WCET tools in your own development?

- Automotive (Engine Control), guiding systems, Automotive control units
- Avionics, On-board SW on satellites
- OS, customer applications
- Synchronous programs
- Embedded controllers
- DSP embedded systems development
- Evaluation of supplier systems

Under which Formal Rules do you work, e.g. DO 178B?

- 5 none
- 4 DO178B,
- US DoD services, NASA
- IEC61508, ...
- ISO9000
- ECSS, usually project-tailored
- DO-248; DO-254; AC 20.115B

- Do you use Coding Guidelines to support WCET analysis?
  - 9 No
  - 3 Yes
- Are you willing to adhere to Coding Guidelines to help WCET analysis?
  - 10 Yes
  - 2 No

10 Yes

Need/Plan to Use

- Processor Architectures with
  - 8 Instruction or data cache
  - 7 Branch Prediction
  - 3 Multi-level cache hierarchy
  - 5 Superscalar out-of-order execution
- Hardware Platforms
  - 4 Mono and multi processor
  - 8 Mono processor

For which Processors would you like to have Timing tools available?

- The usual suspects
  - 7 PowerPC
  - 4 ARM resp. ARM7 and ARM9
  - 3 C166/7
  - Tricore, Coldfire, TMS, sharc, HC12, M16C, TX49,TS101, 68K, MIPS
- Surprises
  - 1 Pentium, 2 x86
  - 2 V850

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For which Target Software Platforms would you like to have Timing Analysis tools available?

- 11 Real-Time OS
- 7 Hardware
- 2 Middleware

III. Current Practice

Do you use tools for Schedulability Analysis?

- 7 Based on Response Time/Rate Monotonic Analysis
- 4 Based on Time Triggered Scheduling
- 1 ARINC 653 (hierarchical model)
- 2 NO TOOL

Do you use tools for WCET Analysis?

- 1 For whole systems
- 1 For parts of the system
- 10 N/A

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Do you use Measuring of the Execution Time to Estimate WCET?

8 Via Code Instrumentation

6 Via Debug Tools (BDM, JTAG, or other)

4 Via Logic Analyzer

Others:

- RTOS includes support
- Chip Internal counter.
- We review suppliers analysis

How much Effort do you spend in Timing Validation?

- 15 % of development
- 5-10 % of development
- 1 % of development
- 9 N/A

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How much Development Time is spent in Measuring the Execution Time of code pieces in addition to Estimating the WCET?

- 10 % of development
- 5 % of development

IV. Requirements

What should be the Functionality of the Tools?

- 6 Very rough first estimate
- 6 Back annotation of results into the source code
- 7 Proposals for cache locking
- 9 Stack-Extent Analysis
- 7 Best Case Execution Time
- 1 Annotated Assembly listing

Other Analyses

- Execution time coupled to its probability
- Average Execution Time
- Assurance of WCET to safety/criticality level required
- Distributions/histograms; indications/estimates of WCET
- Verification of some pre-, postconditions and invariants of functions
- Analyis of code parts with disabled interrupts
- Measurement of OS and communication impact

What is the Tolerable Learning Effort for users of the tool?

- 2 2 days
- 2 3 days
- 1 5 days
- 1 5-10 days

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How much Effort for Annotation of the Code is tolerable?

- 7 Bound for Loops and Recursion
- 3 Locked Cache Contents
- Others:
  - loop bounds often obvious, recursion prohibited at high criticality levels
  - as little as possible
  - as much as possible

What would be Tolerable Analysis Times on realistic code sizes, e.g. 100k instructions?

- 100 000 minutes ☺
- 10 minutes
- 1-10 minutes
- 10-120 minutes
- 60-120 minutes

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Would you adopt a Processor with High Predictability with some loss in average case performance?

(Note, this may mean improved WCET!)

- 9 Yes
- 3 No

Which other Tools should a WCET tool be Integrated with to suit your development flow?

- Enea ASF/DART, some UML-tool
- Ascet SD, Matlab/Simulink
- schedulability, CM, traceability, requirements capture
- WCET and flow analysis must be integrated

Other Remarks

- One respondent is claiming that the questions asked do not fully capture all of the issues due to:
  - different embedded applications with differing needs
  - a WCET prediction should be bound to a level of assurance associated with that prediction
  - predicting WCET should be part of the entire process of developing software, from design to deployment and maintenance

Other Remarks (cont.)

- The faster the analysis time the better, but very tight predictions would be worth several days of analysis time.
- Limiting the scope of processors is reasonable, though it limits the market in which a timing analysis tool can be applied.
- Limiting the language of programs being analyzed is reasonable, though some users may complain.
- The price of a timing analysis tool is a very sensitive issue since it can affect the viability of the product.

Other Remarks (cont.)

- The tools should be automated and should require little or no user intervention.
- Timing analysis tools should be complemented with stress testing, presumably due to WCET tools not being completely reliable.
- There are many complicated architectural features that are difficult to analyze, which include DMA and bus arbitration in complex multi-DSP systems.
- Some vendors rely on suppliers to provide WCET information that can be used in certification efforts.

What is the maximum tolerable price per seat for such a tool

(under the assumption that its use saves money spent in validation otherwise) ?

- 1 up to 10000 $
- 7 up to 5000 $
- 1 up to 50000 $
- 3 Don't know

Conclusions

- WCET Prediction is important.
  - willingness to sacrifice performance for predictibility
- Future Issues
  - interaction with energy awareness
  - extending WCET determination to high-level design